♦ FOUNDRY SERVICE

Foundry services have been one of the core businesses at SEI, providing sophisticated GaAs IC technology for all customers. SEI offers very flexible service to support the customers own circuit designs. For information on SEI's foundry services, an additional summary book specifically on SEI's foundry services is available for all customers.

• *SEI's FEATURE*

SEI provides two choices from the fabrication process based on ion-implantation technology and epitaxial technology as shown in Fig. 1-6-1. The basic process flow is the single-layer resist dummy-gate self-aligned process (SRD), being matured as a completely ion-milling process for two-layer metals. SEI has achieved a very narrow sawing line width of 70 mm to harvest more chips across a wafer as well as highly uniformity and excellent reproducibility. SEI serves a quick delivery of typical eight weeks from customer's mask-out and flexible delivery options.

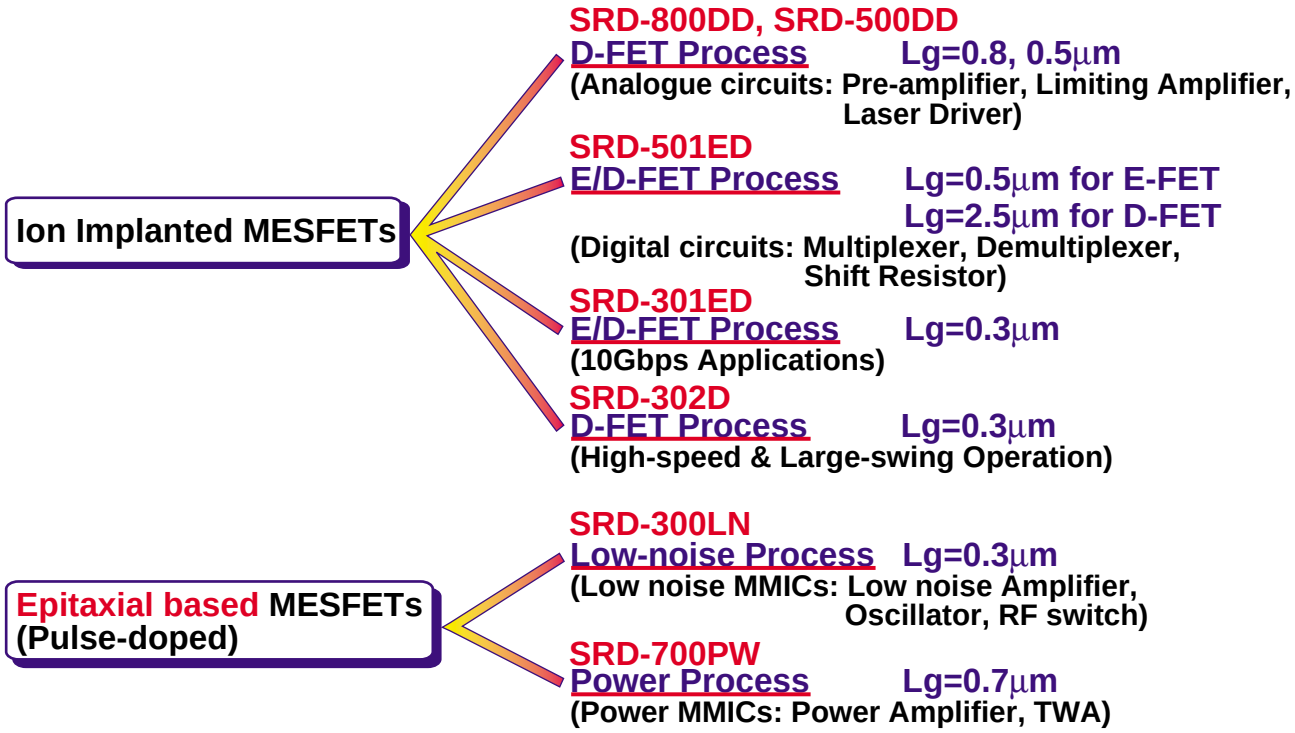


Fig. 1-6-1 : GaAs IC Process Lineup

Foundry Program

SEI's Foundry Services provide experienced designers with the opportunity to design and lay out their own GaAs integrated circuits and to have these circuits processed by SEI utilizing state-of the art wafer processing facilities and production-proven technology.

As part of the program, SEI transfers a comprehensive design documentation package including circuit layout design rules, and device characteristics. Other CAD services such as Design Rule Checking are also available.

The SEI foundry program offers a complete range of tools and services to accommodate a customer's particular requirements. Customers can transfer CALMA GDS II tapes and have SEI fabricate masks. Foundry wafer acceptance is based on test results of the universal process control monitor (PCM) test patterns which are situated on the right side and lower side of every reticle field. Target values for selected PCM test parameters are shown in the Foundry Services data sheet.

Foundry Flow

SEI normally supports the conventional service where the customer provides his own design in the form of computer tapes. The foundry delivers the wafer, or performs dicing and DC testing, if necessary. The customer provides his original design by the GDS II tape, and SEI performs the wafer fabrications, and delivers the wafer to the customer. The foundry flow is shown in Fig. 1-6-2.

Complete support is provided for all customers and a foundry manual is also prepared to help the customer's design. Typical FET parameters to need to the circuit design and the layout design rules are presented in the foundry manual which is available only for customers who are licensed under an initial contract. Additional information, especially the FET parameters for the circuit design, which is not described in the foundry manual, often will be needed for individual design for each customer. SEI can offer most of the required data to the customer and would like to measure to the extent possible.

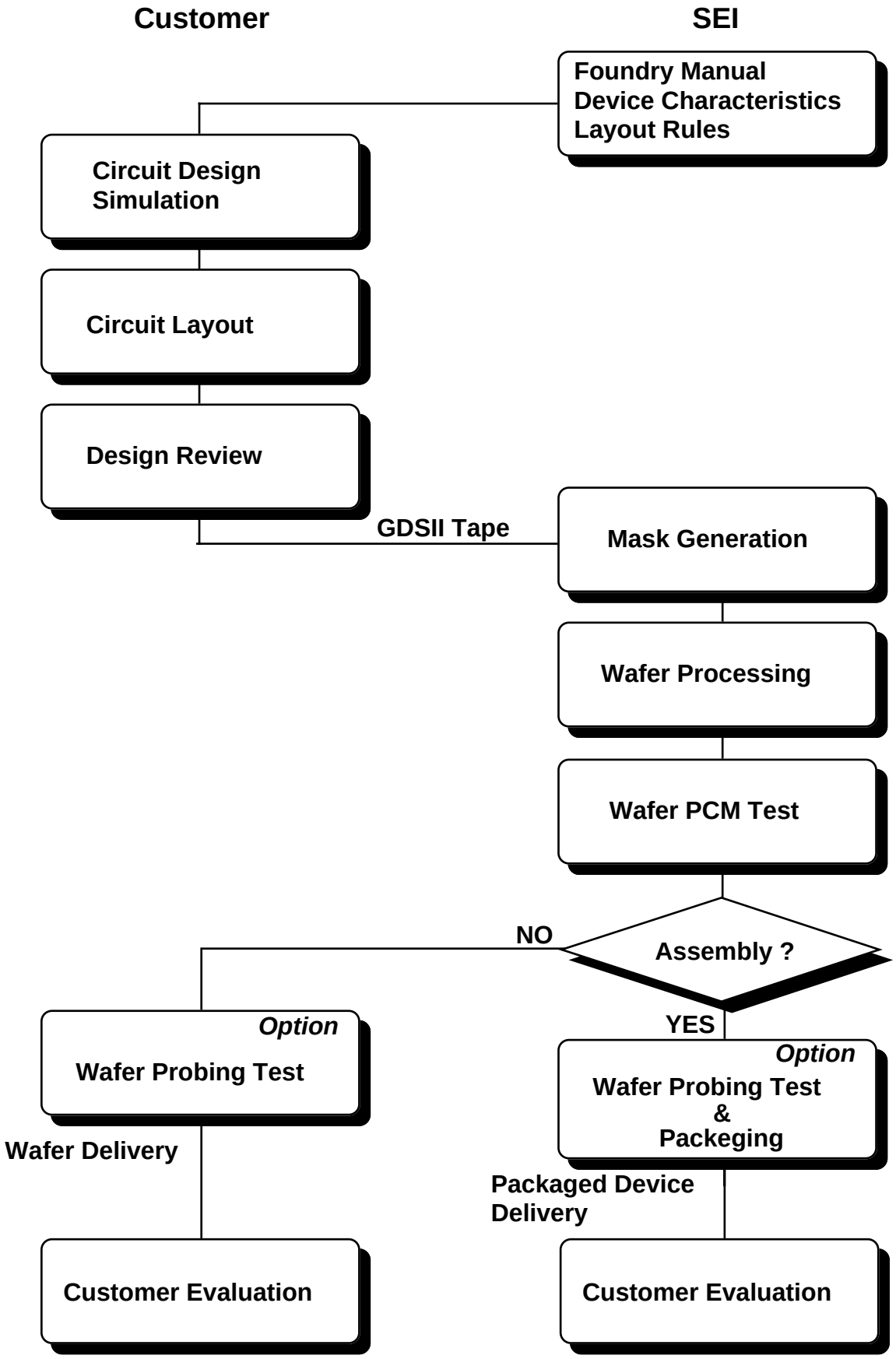


Fig. 1-6-2 : Foundry Flow

Foundry Menu

SEI's foundry menu is classified into two major device technologies; one is based on ion-implanted MESFET technology and the other is the "Pulse-doped MESFET process" based on epitaxial technology. Both technologies are originally developed by SEI and the fabrication process is basically "SRD" as previously described. Table 1-6-1 shows the SEI foundry menu. All processes use 3-inch wafers at present and the extended line for 4-inch wafers will be planned to start at the beginning of 1999.

An overview of the application area of SEI's foundry service is shown in Fig. 1-6-3. The SRD-700PW and SRD-300LN are based on the pulse-doped MESFET technology; the details of the applications and features are shown in the SEI data book for wireless devices. The SRD-700PW is a power FET process with the gate length (Lg) of 0.7 mm applicable for use in mobile communications systems and so on up to 5 GHz, and the SRD-300LN is a low noise MESFET process with the Lg of 0.3 mm applicable for use in wireless systems up to 30 GHz, as shown in Fig. 1-6-3.

Other processes are based on the ion-implanted MESFET technology. The SRD-800DD based on 0.8 mm devices and SRD-500DD based on 0.5 mm devices are the lineups applicable for various analog circuits such as high speed optical communications system up to 5 Gbps, allowing the design flexibility of circuit configuration owing to dual threshold voltages

Table 1-6-1 : SEI's Foundry Menu

Process	Structure	Gate Length	Vth (V)	Feature
SRD-700PW	MBE (OMVPE)-grown Advanced Pulse-doped Asymmetric Self-aligned LDD	0.7μm	-2.2V	High Vb> 15V Low-Distortion f_T=10GHz
SRD-300LN	MBE (OMVPE)-grown Pulse-doped Self-aligned LDD	0.3μm	-1.0V	Low-Noise NF=1.0dB@12GHz f_T=32GHz
SRD-800DD	Direct Ion-implanted Self-aligned LDD	0.8μm	-0.4V	Highly uniform σ Vth < 25mV f_T=26GHz/0.5μm
SRD-500DD		0.5μm	-1.0V	
SRD-501ED	Direct Ion-implanted Self-aligned LDD	0.5μm for E	-0.4V	Highly uniform σ Vth < 25mV f_T=28GHz
		2.5μm for D	-1.0V	
SRD-301ED (Preliminary)	Direct Ion-implanted Self-aligned Advanced LDD	0.3μm	0V/E -0.4V/D	Highly uniform σ Vth < 50mV f_T=40GHz
SRD-302D (Advance)	Direct Ion-implanted Asymmetric Self-aligned LDD	0.3μm	-1.0V	High-speed & Large-swing Operation Vb >12V, f_T=20GHz

of -0.4 V and -1.0 V. The SRD-501ED is the menu for logic circuits with the clock frequency upto 5 GHz, consisting of 0.5 mm enhancement mode FET's (E-FET) and 2.5 mm depletion mode FET's (D-FET). The SRD-301ED is the new process based on 0.3 mm devices. It can be applied to the design analog and digital circuit for the 10 Gbps system, be and has already been available.

The SRD-302D is the latest process based on 0.3 mm devices in the final stage of development. The differnce between the SRD-301ED and SRD-302D is the break down voltage. While the SRD-302D is applied the same 0.3 mm technology as the SRD-301ED, the break down voltage was greatly improved by a little change of the device structure. Recently there has beeb a growing demand by high-speed and large-swing operation. The SRD-302D having the breakdown voltage as high as 12 V is optimum process for such applications and will be released soon.

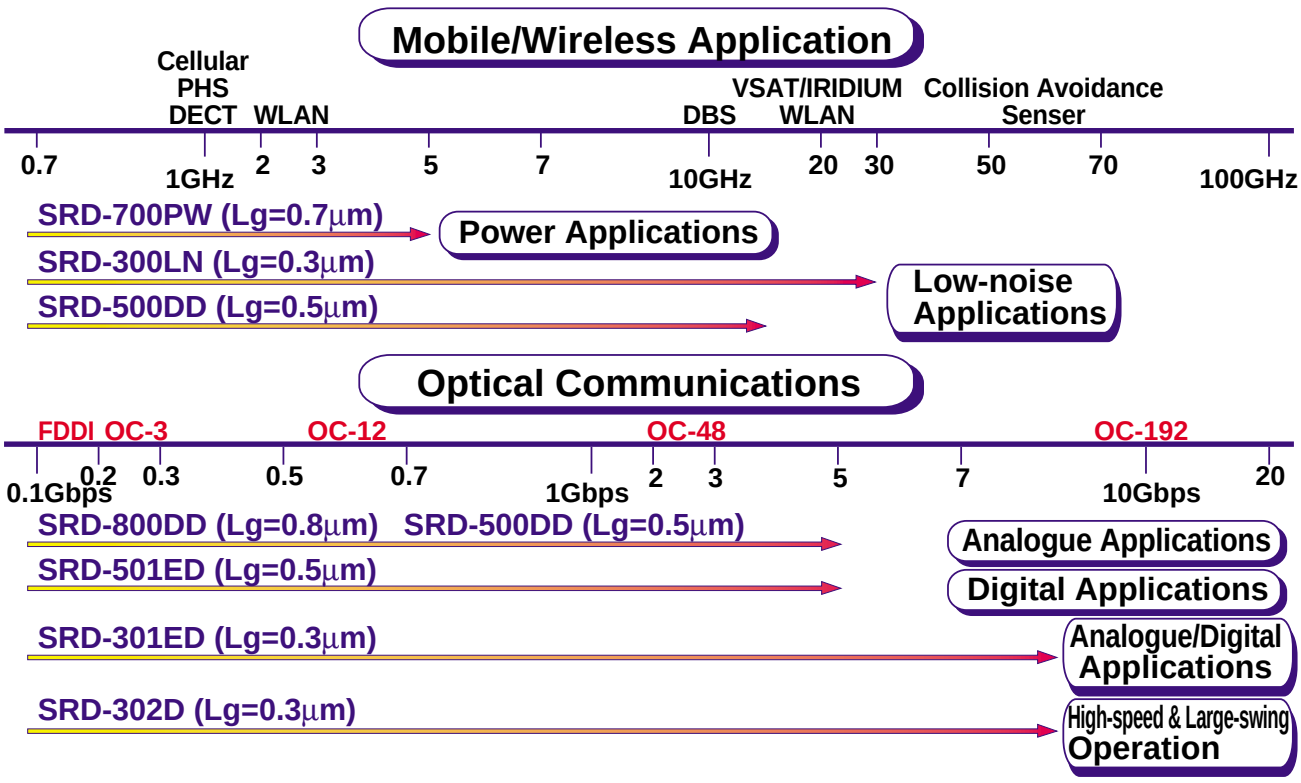


Fig. 1-6-3 : Overview of Application Area in SEI's Foundry Menu

Standard IC Structure

SEI IC's are based on MESFET's and Schottky barrier diodes. Planar circuits are fabricated by using multiple, selectively masked ion implants in semi-insulating GaAs substrates. LDD (Lightly Doped Drain) self-aligned gate structure by using the dummy gate process offers high performance and good uniformity of device characteristics. Direct step on wafer (DSW) 10x reduction projection photolithography is used for delineated a circuit patterns. Pattern replication is accomplished with dry processing techniques. The standard process includes two levels of metal interconnection. The first level interconnection and Schottky metal are completed in a different metallization step. The first level interconnection is placed on dielectric film. The first and second level interconnections are separated from each other by an interleave dielectric. A summary of fabrication techniques used in SEI's standard IC process is listed in Table 1-6-2. Table 1-6-3 shows a summary of interconnection.

Table 1-6-2 : Summary of Standard IC Process

PROCESS STEP	MATERIALS	FABRICATION TECHNIQUE
Device		
Active Device Regions	Si (n-type) on Implantation Be Ion Implantation for buried P-Laver	Multiple Selective Implants
Thin Films		
Dielectrics : Anneal cap	SiN	Plasma Enhanced CVD
Pattern Inversion	SiO_2	Sputtered
1st level	SiON	Plasma Enhanced CVD
Interlevel	SiON	Plasma Enhanced CVD
Passivation	SiON/SiN	Plasma Enhanced CVD
Matallizations		
Ohmic Contacts	AuGe/Ni	E-Beam Evaporation
Gate	Ti/Pt/	E-Beam Evaporation
1st level	TiW/Au	Sputtered
2nd level	TiW/Au	Sputtered
Lithography		
Resist Delineation	Positive Resist	10×DSW Projection Photolithography
Pattern Replication	Dielectrics	Reactive Ion Etching
	Ohmic Contacts	Enhanced Lift-off
	Gate	Enhanced Lift-off (Tri-level resist)
	1st Level	Ion Milling
	2nd Level	Ion Milling

Table 1-6-3 : Summary of Interconnection

Process	Structure	Thickness	Line & Space	Reference
Gate	Evaporated & Lift-off Ti/Pt/Au	2900Å		General Purpose
	Evaporated & Lift-off Ti/Pt/Au	7400Å		For MMIC
1st level	Sputtered & Milling TiW/Au	5500Å	2.0µm/2.0µm	Analog/Digital Circuit
	Evaporated & Lift-off Ti/Pt/Au	6900Å	0.5µm/1.5µm	High Current Derivability
2nd level	Sputtered & Milling TiW/Au	6500Å	2.0µm/2.0µm	Analog/Digital Circuit
	Sputtered & Milling TiW/Au	10000Å	3.0µm/3.0µm	High Current Derivability
	Evaporated & Milling Ti/Pt/Au	30000Å	8.0µm/8.0µm	For MMIC

Maximum current density is 2E5 A/cm^2

• *TYPICAL PROCESS PROFILE* - ION-IMPLANTATION TECHNOLOGY

Typical process profiles of SRD-800DD, SRD-500DD, SRD-501ED, SRD-301ED, and SRD-302D are shown in Figs. 1-6-4 to 1-6-8.

Devices

Self-Aligned LDD MESFET
SBD
Implanted Resistor
MIM Capacitor

Interconnections

SOG Planarization
Sputtered TiW/Au
Ion Milling
1st level 2.0μm L&S
2nd level 3.0μm L&S

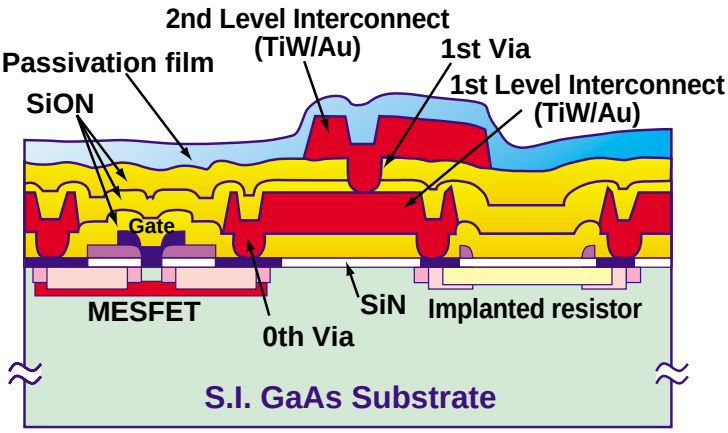


Fig. 1-6-4 : SRD-800DD

Typical Device Parameters

	D1-FET	D2-FET
Vth (mV)	-400	-1000
σVth (mV)	20	20
Idss (mA/mm)	38	150
gm (mS/mm) @Vg=0V	160	230
Vbd (V) @1μA/μm	-8	-6
f_T (GHz) @Vg/0V	16	18

Applications

Limiting Amplifier
Laser Diode Driver
and so on.

Devices

Self-Aligned LDD MESFET
SBD
Implanted Resistor
MIM Capacitor

Interconnections

SOG Planarization
Sputtered TiW/Au
Ion Milling
1st level 2.0μm L&S
2nd level 3.0μm L&S

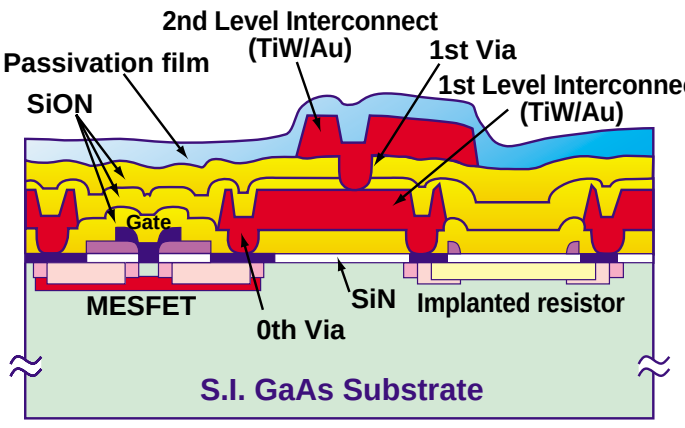


Fig. 1-6-5 : SRD-500DD

Typical Device Parameters

	D1-FET	D2-FET
Vth (mV)	-500	-1100
σVth (mV)	30	30
Idss (mA/mm)	65	200
gm (mS/mm) @Vg=0V	210	250
Vbd (V) @1μA/μm	-8	-6
f_T (GHz) @Vg/0V	25	26
NF/Ga (dB) @4GHz		0.6/13.0

Applications

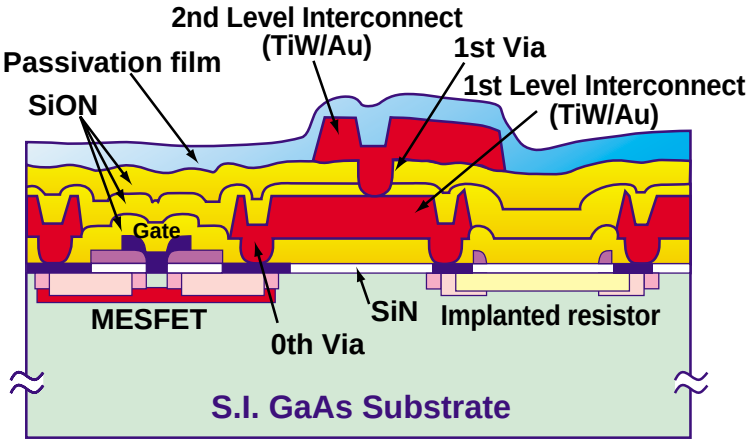
Limiting Amplifier
Laser Diode Driver
L-band Low Noise
and so on.

Devices

Self-Aligned LDD MESFET
SBD
Implanted Resistor
MIM Capacitor

Interconnections

SOG Planarization
Sputtered TiW/Au
Ion Milling
1st level 2.0μm L&S
2nd level 3.0μm L&S



Typical Device Parameters

	E-FET	D-FET
Lg (μm)	0.5	2.5
Vth (mV)	100	-450
σVth (mV)	20	20
Idss (mA/mm)	85*	25
gm (mS/mm)	300*	100
Vbd (V) @1μA/μm	-5	-4
f_T (GHz)	28*	

*Vg=0.6V

Applications

MUX/DEMUX
T-FF/D-FF

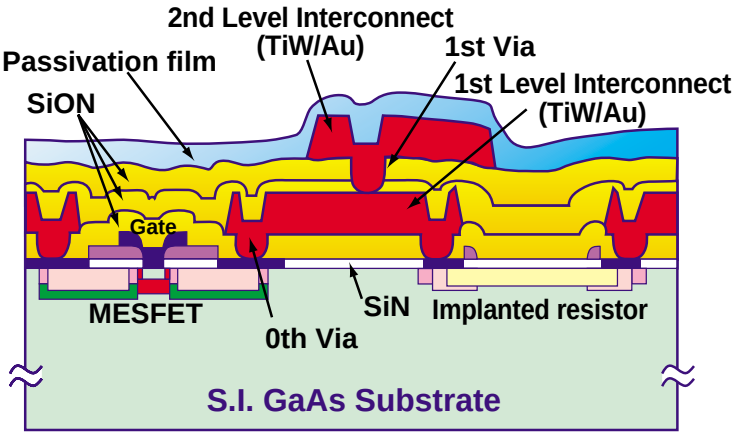
Fig. 1-6-6 : SRD-501ED

Devices

Self-Aligned Advanced LDD MESFET
SBD
Implanted Resistor
MIM Capacitor

Interconnections

SOG Planarization
Sputtered TiW/Au
Ion Milling
1st level 2.0μm L&S
2nd level 3.0μm L&S



Typical Device Parameters

	E-FET	D-FET
Lg (μm)	0.3	0.3
Vth (mV)	0	-400
σVth (mV)	40	50
Idss (mA/mm)	125*	100**
gm (mS/mm)	420*	300**
Vbd (V) @1μA/μm	-7	-5
f_T (GHz)	45*	40**
NF/Ga (dB) @12GHz		1.1/8.5

* Vg=0.6V ** Vg=0V

Applications

High Speed
Digital/Analog Circuits

Fig. 1-6-7 : SRD-301ED

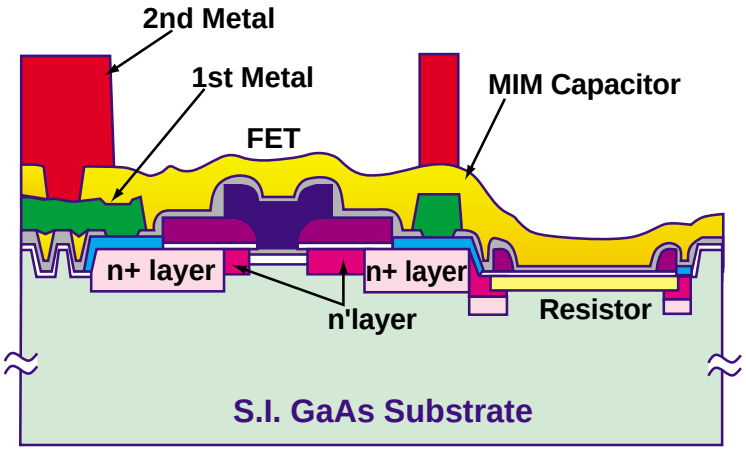
Devices

Asymmetric Self-aligned LDD MESFET
SBD
Implanted Resistor
MIM Capacitor

Interconnections

Sputtered TiW/Au
1st level 2.0μm L&S

Electro-plating Au
2nd level 8.0μm L&S



Typical Device Parameters

Lg (μm)	0.3
Vth (V)	-1.0
σVth (mV)	50
Idss (mA/mm)	200
gm (mS/mm) @Vg=0V	260
Vbd (V) @0.5μA/μm	-12
f_T (GHz)	20

Applications

High-speed & Large-swing Operation
Drive FET/High Power Amp.

Fig. 1-6-8 : SRD-302D

• *TYPICAL PROCESS PROFILE* - EPITAXIAL TECHNOLOGY

Typical process profiles of SRD-700PW and SRD-300LN based on "Pulse-doped MESFET Technology" are shown in Figs. 1-6-9 and 1-6-10.

Devices

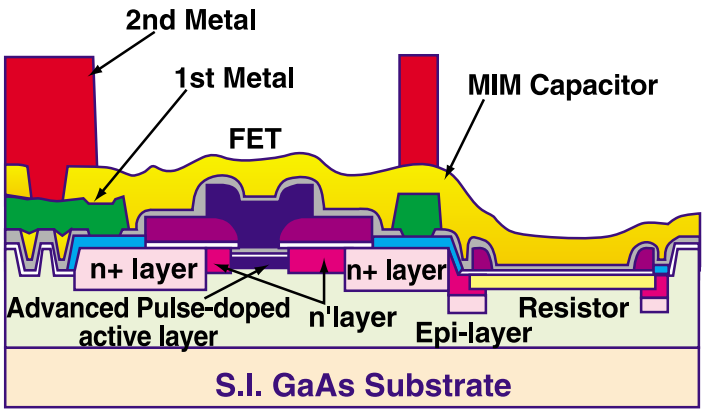
Advanced Pulse-doped
Asymmetric Self-aligned LDD MESFET
Implanted Resistor
MIM Capacitor

Interconnections

Electro-plating Au
1st level 1.5μm L&S
2nd level 8.0μm L&S
70μm wafer thickness

Typical Device Parameters

Vth (mV)	-2.2
σ Vth (mV)	100
Idss (mA/mm)	250
gm (mS/mm) @Vg=0V	120
Vbd (V) @0.5μA/μm	-15
f_T (GHz)	10
P1dB (dBm) @1.9GHz, Wg=5.2mm	31
Efficiency (@6V)	43%
ACP (600KHz)	-60dBC



Applications

High Power Amp.
Highly Linear Amp.

Fig. 1-6-9 : SRD-700PW

Devices

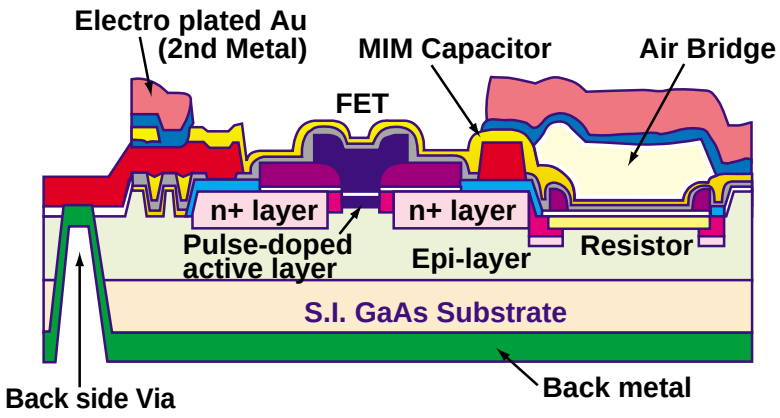
Pulse-doped
Self-Aligned LDD MESFET
Implanted Resistor
Spiral Inductor
MIM Capacitor

Interconnections

Electro plated Au
Air Bridge
1st level 1.5μm L&S
2nd level 8.0μm L&S
100μm wafer thickness
Back-side Via

Typical Device Parameters

Vth	-1.0
σVth (mV)	50
Idss (mA/mm)	210
gm (mS/mm) @Vg=0V	280
f_T (GHz) @Vg/0V	30
NF/Ga (dB) @12GHz	1.0/8.0



Applications

K-band Low Noise Amp.

Fig. 1-6-10 : SRD-300LN