♦ FABRICATION PROCESS TECHNOLOGY

SEI originally developed the sophisticated GaAs metal semiconductor field effect transistor (MESFET) process of IC's for use in high-speed optical communications systems. To realize low cost and high volume GaAs IC production, requires the uniformity of device characteristics from wafer to wafer as well as across a wafer. The self-aligned gate structure has been established as the best technology to obtain excellent device performance and highly uniform characteristics across the wafer. SEI provides the manufacturable self-aligned lightly-doped drain (LDD) GaAs MESFET based on a single resist-layer dummy-gate (SRD) process. The fabrication process of the pulse-doped MESFET for wireless devices is also based on the SRD.

SEI provides various GaAs IC's for use in high-speed optical communications systems. The lineups cover the data communications system with the data rate up to a couple of hundred-Mbps and the telecommunications system with the transmission speed up to 10 Gbps, featuring low-noise performance in the receiver circuits and excellent waveshape in the driver circuits. Customers can choose bare chips, plastic molded packages, metal hermetic-sealed packages, and so on for use. All customers can develop the original GaAs IC's using the SRD process because SEI prepares the foundry service with the standard.

• *SRD*

The GaAs MESFET in the SRD process has a buried p^- layer lightly doped drain (BPLDD) structure as shown in Fig. 1-2-1. The main SRD process flow is shown in Fig. 1-2-2. Undoped LEC 3-inch substrates are selectively implanted with 70 KeV Be^+ and 30 KeV Si^+ to form the device active regions. A fully depleted BP-layer was adopted to prevent the increased parasitic capacitance. After deposition of plasma enhanced chemical vapor deposition (PE-CVD) 800 Å SiN film, a 1.6 mm thick photoresist, which acts both as an ion stopping mask during implantation and dummy gate, is patterned by an i-line stepper. For n^+ layer formation, high-dosage Si^+ implantation is carried

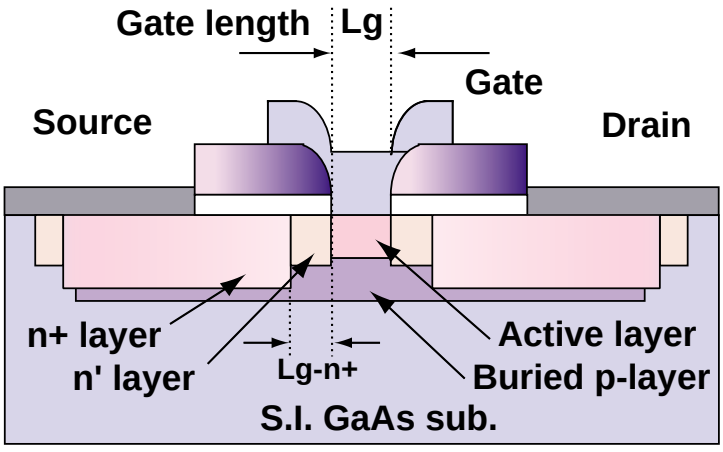

Fig. 1-2-1 : SRD Device Structure

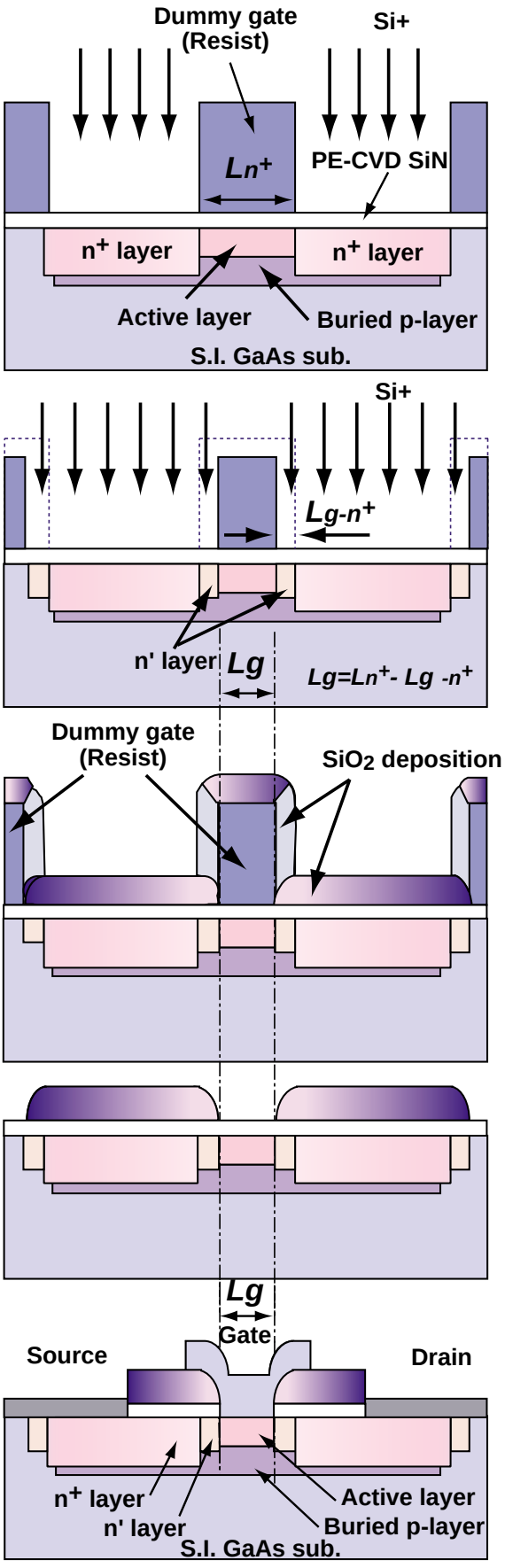

Fig. 1-2-2 : SRD Process Flow

out at 90 KeV through the SiN film. After the photoresist is reduced by O_2 plasma etching, Si+ is implanted at 50 KeV through the SiN film for n'-layer. The dummy gates are substituted with sputtered 3000 Å SiO_2 film. The SiO_2 adhering to the side wall of the photoresist can easily be removed in a buffer-HF solution. After lifting off the undesired photoresist and SiO_2, electrical activation is performed at 800 °C for 20 minutes in N_2 ambient. After opening the source/drain regions by reactive ion etching (RIE), the AuGe/Ni is evaporated and alloyed for ohmic contact.

The gate electrode regions are patterned using tri-level resist, opened by CF_4 RIE when the SiO_2 acts as an etching mask, and then Ti/Pt/Au is evaporated and lifted off. The gate metal overlaps the SiO_2-SiN film by 0.3 μm on each side to keep alignment margins. Isotropic etching for the photoresist is one of the key technologies. Figure 1-2-3 shows the photoresist etching characteristics. By optimizing the pressure and RF power of the parallel plate type etching apparatus, SEI suc-

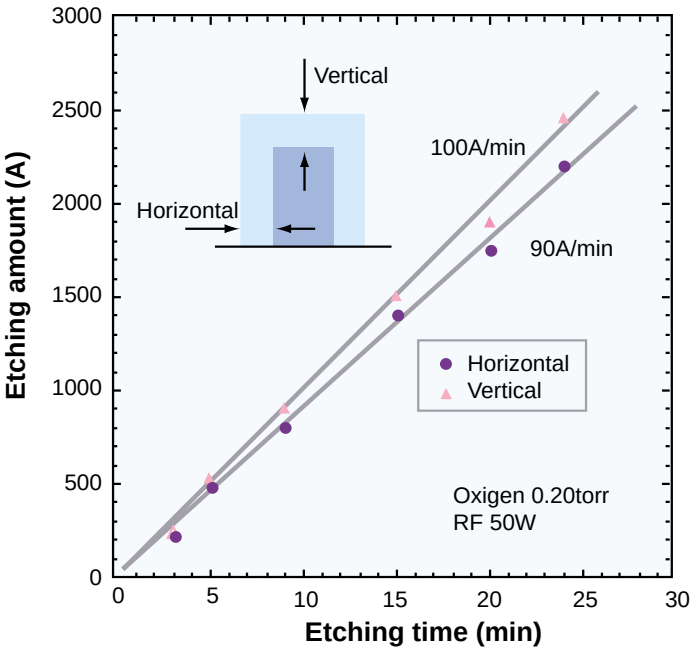

Fig. 1-2-3 : Photoresist Etching Characteristics using O_2 Plasma

cessfully obtained good controllability of etching characteristics. The photoresist maintains sufficient thickness to act as an ion-stopping mask after etching. In addition, the photoresist maintains clear rectangularity during the n^+ process, which is important to control the pattern inversion by SiO_2 deposition and lift-off.

Determination of Production Standards

To obtain uniform device characteristics from wafer to wafer, SEI determined the control standard of several parameters. In the SRD process, n^+ and n'-layers are formed by implantation through SiN , so the thickness of the SiN film affects the sheet resistance of these layers. The production standard of SiN film thickness was 800±80 Å, which could control the sheet resistance of the n^+ layer at 265±10 Ω/□. It is well known that device characteristics are affected by the gate length (Lg), n^+ spacing (Ln^+), and the spacing between the n^+/gate edge ($Lg\text{-}n^+$) which corresponds to the side etch amount of the dummy-gate (see Fig.1). First, the effect of Ln^+ on Vth was investigated.

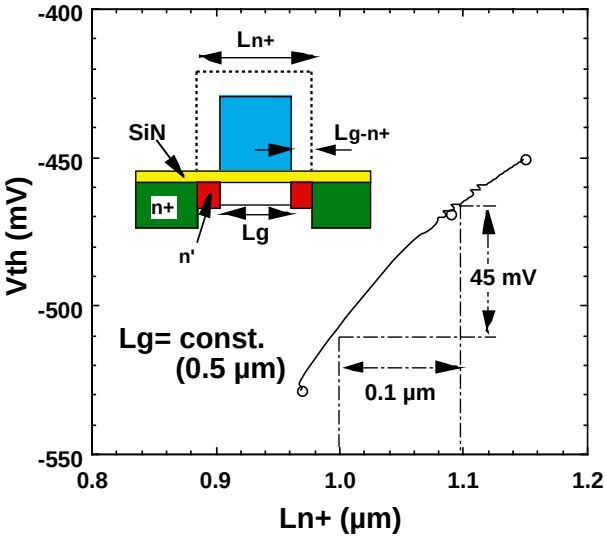

Fig. 1-2-4 : Ln^+ Dependence on Vth for 0.5μm Devices

Figure 1-2-4 shows the Ln^+ dependence on the Vth for 0.5 μm devices. As shown in Fig. 1-2-4, the Lg is constant so the $Lg\text{-}n^+$ is changed. The Vth has little dependence on the Ln^+. The effect of $Lg\text{-}n^+$ on the breakdown voltage (Vb) and the drain conductance (gd) as shown in Fig. 1-2-5 were investigated as well. The Vb and gd strongly depend on the $Lg\text{-}n^+$. In analogue circuits, these characteristics affect the bandwidth, gain, sensitivity, and so on. From these results, SEI found that the $Lg\text{-}n^+$ should be controlled rather than the Ln^+ . Therefore, the production standards of Ln^+ and $Lg\text{-}n^+$ to be 1.10±0.0 4 mm and 0.30±0.015 μm, respec-

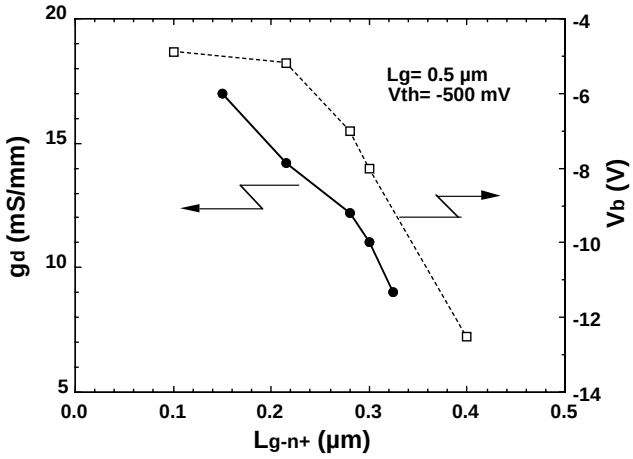

Fig. 1-2-5 : $Lg\text{-}n^+$ Dependence on Vb and gd

tively were determined for a 0.5 μm device. When the Lg-n^+ is 0.30 μm, the voltage gain (gm/gd) maximizes.

DC Characteristics

The DC parameters are taken on 20 μm-wide process control monitor (PCM) FET's at 37 locations uniformly distributed across each wafer. Figure 1-2-6 shows the Vth dependence on the drain saturation current (Idss). The Idss was determined by only the Vth, which suggests that Schottky characteristics and K-values are very stable from wafer to wafer.

Figure 1-2-7 shows the Vth and standard deviation of Vth (σVth) histograms where the Si^+ dose is constant ($4.2\times10^{12}/cm^2$) for each wafer. The controllability of Vth from wafer to wafer is within ±50 mV and the σVth across the wafer is less than 30 mV for 0.5 mm devices.

The Vb was controlled at -8.0±1.5 V for the devices of -500 mV Vth.

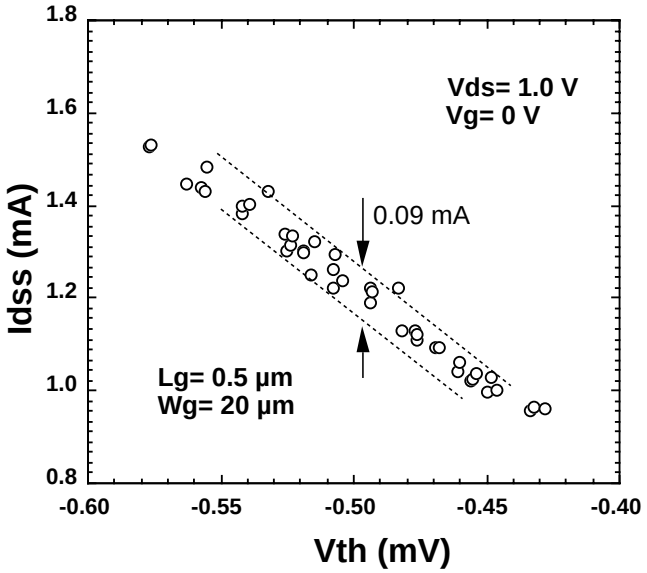

Fig. 1-2-6 : Vth vs. Idss for 0.5 μm Devices

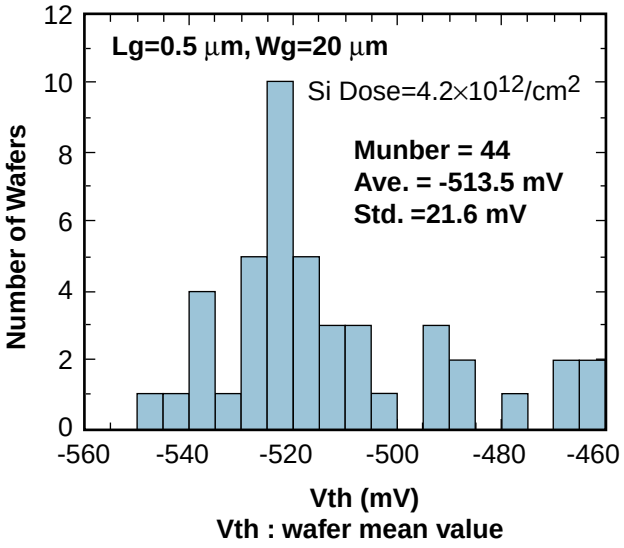

Fig. 1-2-7(a) : Histogram of Vth from Wafer to Wafer

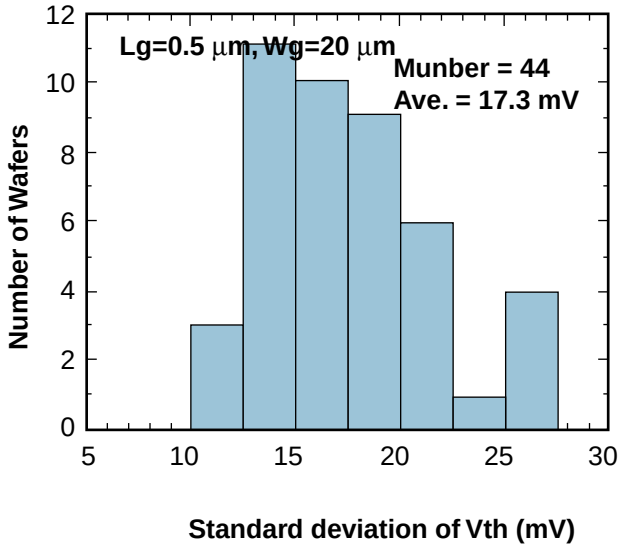

Fig. 1-2-7(b) : Histogram of σVth across a Wafer

RF Characteristics

S-parameters were measured by using Cascade probes and HP-8510B on 200 μm-wide FET's. The bias conditions are Vds=2.0 V and Vg=0 V. The equivalent circuit elements are deduced from the measured S-parameter. Figure 1-2-8 shows the statistical process control charts of gm, Rds (=1/gd), and current gain cutoff frequency (f_T) . From these figures, gm and gd control are very good, within ±7 % (Max-Min) from the designed values. The control f_T is also very good.

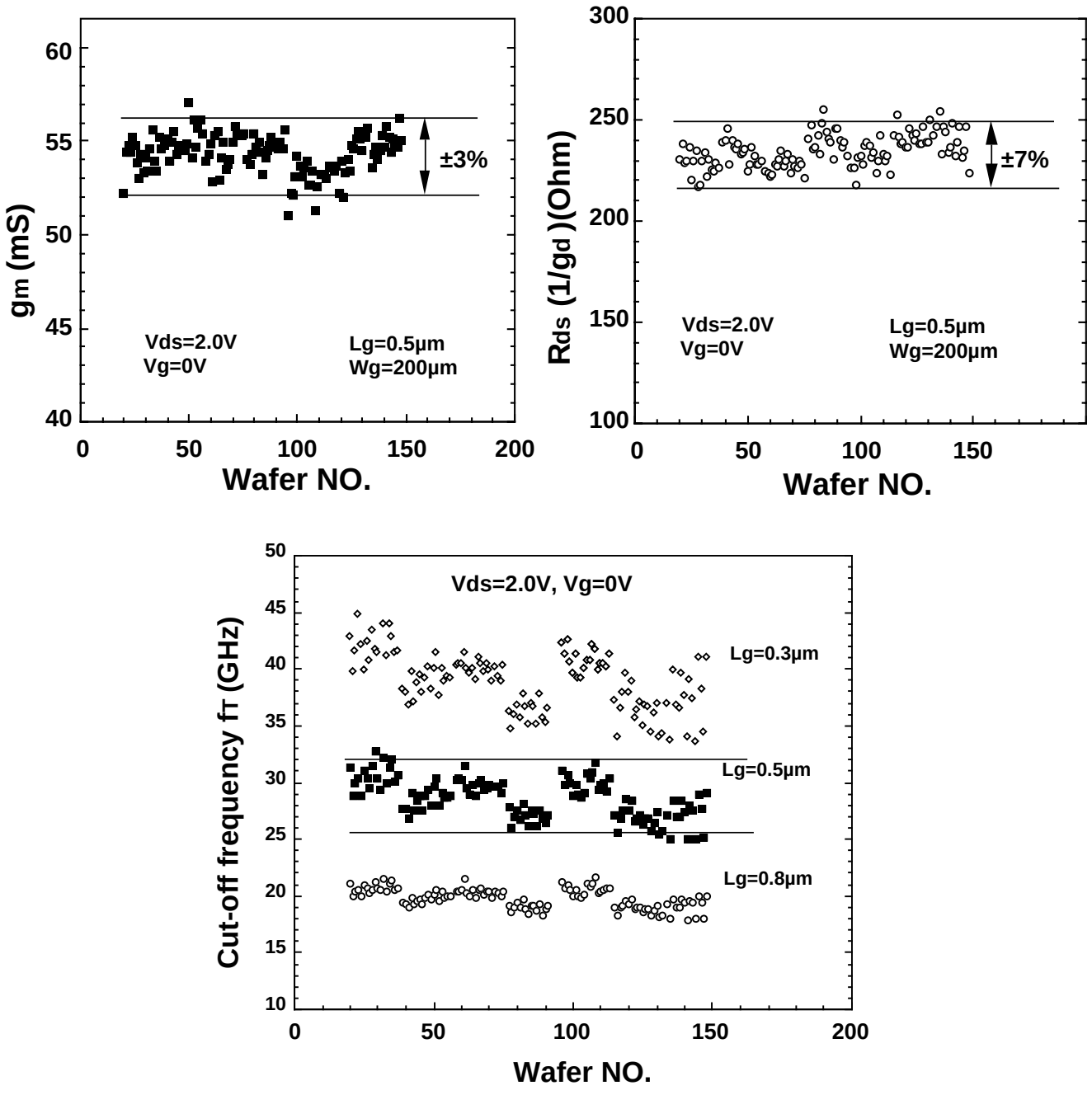

Fig. 1-2-8 : Statistical Process Control Charts of gm, Rds, and f_T

Under the short channel approximation, f_T is determined by the following equation,

$$f_T = Vs / 2\pi Lg$$

where Vs is saturation velocity and assumed to be 1.0×10^7 cm/sec. Assuming that the deviation of f_T is attributed to the deviation of Lg, we can deduce the deviation of Lg to be ± 0.05 μm which corresponds to the production standard of Ln^+.

• *IC IMPLEMENTATION*

Two kinds of Vth are used to improve the circuit performance. A GaAs IC includes an ion-implanted resistor, two-level interconnection fabricated by sputtered TiW/Au and ion-milling, and metal-insulator-metal (MIM) capacitor where SiON is used as the insulator. Figure 1-2-9 shows the schematic cross section of GaAs IC. The typical device parameters and the interconnection design rules are summarized in Table 1-2-1. SEI has been successfully fabricating various kinds of GaAs IC's for optical communications systems using the SRD process.

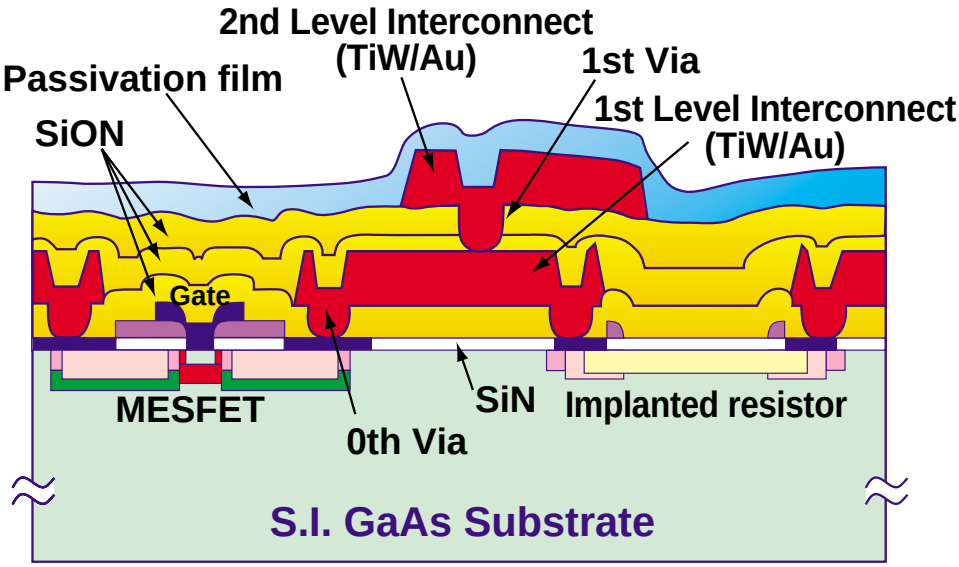

Fig. 1-2-9 : Schematic Cross Section of GaAs IC

Table 1-2-1 : Typical Device Parameters and Interconnection Design Rules

Device Prameeters

	D1-FET	D2-FET
Vth(mV)	-500	-1100
Idss(mA/mm)	62	190
fT(GHz)	26	26

Interconnection Design Rules

Metal Layer	Line/Via	Space
0thVia	1.2 1.2 m	1.2 m
I1st Lavel	1.5 m	1.5 m
1st Via	1.2 1.2 m	1.2 m
2nd Lavel	2.0 m	2.0 m