♦ WIRELESS DEVICE TECHNOLOGY

SEI originally developed the sophisticated GaAs metal semiconductor field effect transistor (MESFET) process of IC's for use in high-speed optical communications systems. To achieve low cost and high volume GaAs IC production, requires the uniformity of device characteristics from wafer to wafer as well as across a wafer. The self-aligned gate structure has been established as the best technology to obtain excellent device performance and highly uniform characteristics across the wafer. SEI provides the manufacturable self-aligned lightly-doped drain (LDD) GaAs MESFET based on a single resist-layer dummy-gate (SRD) process.

SEI offers various GaAs IC's for use in high-speed optical communications systems. The lineups cover the data communications system with a data rate up to a couple of hundred-Mbps to the telecommunications system with the transmission speed up to 5 Gbps, featuring low-noise performance in the receiver circuits and excellent waveshape in the driver circuits. Customers can choose bare chips, plastic molded packages, metal hermetic-sealed packages, and so on for use. Customers can develop the original GaAs IC's using the SRD process because SEI prepares the foundry service with the standard.

The SRD process is detailed in the previous chapter. This chapter describes the details of "advanced pulse-doped MESFET" as shown in Fig. 1-3-1.

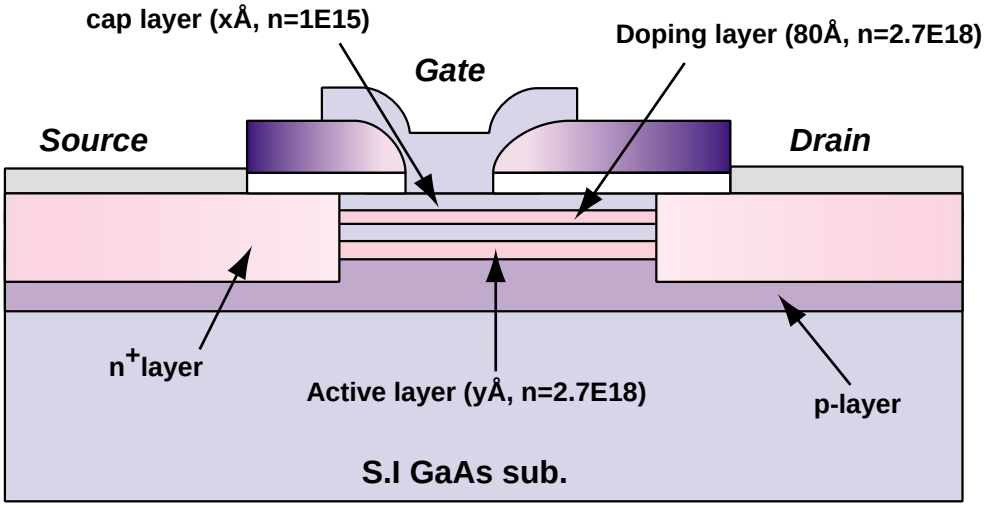

Fig. 1-3-1 : Structure of an Advanced Pulse-doped MESFET

• *ADVANCED PULSE-DOPED MESFET*

A pulse-doped MESFET with a highly doped and thin active layer is highly suitable for low distortion power application because of its intrinsic characteristics of good linearity. Power FETs mostly have a recessed gate structure to improve their breakdown voltage, resulting in poor uniformity and poor reproducibility of device performances because of the unsatisfactory controllability of recess etching.

An advanced pulse-doped MESFET as shown in Fig. 1-3-1 has been developed to solve the above problems and simultaneously achieve good linearity of device performance. Besides a pulse-doped active channel, another pulse-doped layer has been incorporated between the active channel and gate electrode. Doping density and thickness of the incorporated pulse-doped layer are designed so that the surface depletion layer does not extend into the active channel. This is the same function as the recessed structure and avoids the long-gate effect, which improves linearity of a pulse-doped MESFET without a recessed structure.

To achieve a high gate-drain breakdown voltage (V_{BD}) without a recessed gate structure, a two-dimensional device simulator was used to design the device structure. Furthermore, a new process technology for the lightly doped drain (LDD) structure was developed to simultaneously achieve low source resistance and high source-drain breakdown voltage.

Device Design

Electric field distribution in a MESFET was calculated by the simulator. Electric field (EF) included both horizontal (E_x) and vertical (E_y) components {$EF=(Ex^2+Ey^2)^{1/2}$}. Figure 1-3-2 shows the simulation results for a MESFET with a cap layer of 600 Å at a drain-source voltage (Vds) of 6 V and Vg of 0 V. Simulation findings indicated that the thickness of an undoped GaAs cap layer affected the electric field more than any other parameter.

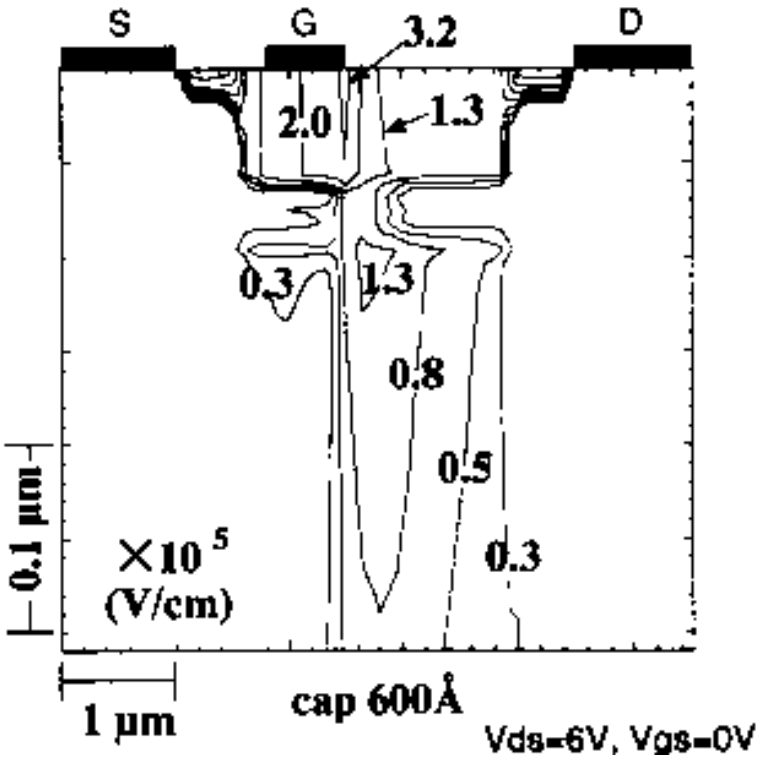

Fig. 1-3-2 : Simulation Results of Cross-sectional Electric Field of MESFET

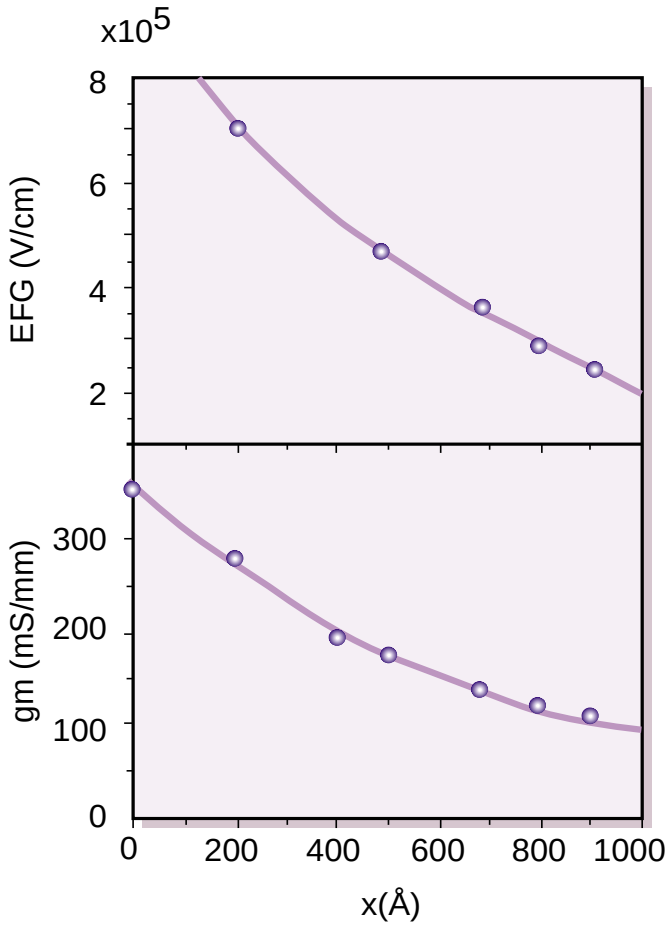

Fig. 1-3-3 : Electric Field and gm Dependence on Thickness (x) of GaAs-cap Layer (Simulation)

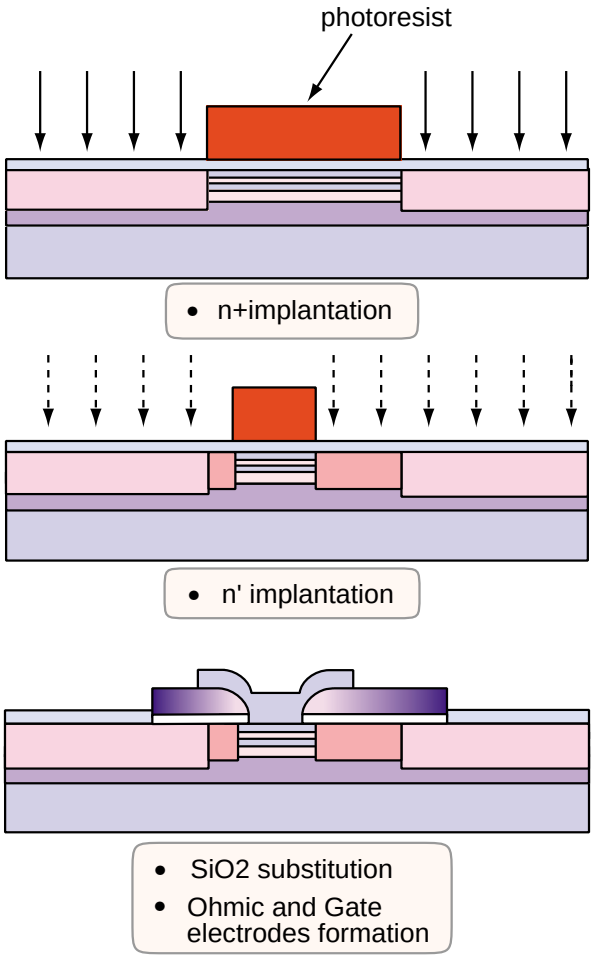

Fig. 1-3-4 : Fabrication Procedure of LDD Structure

Electric field of the drain edge of the gate (EF_G) was adopted to estimate V_{BD}. Figure 1-3-3 shows the relationship between EF_G and thickness of a GaAs cap layer (x). Figure 1-3-3 also includes the dependence of the calculated transconductance (gm) on x. Since EF_G decreased as x became thicker, V_{BD} was expected to be higher. But gm steadily decreased as x became thicker. Therefore, the thickness of a GaAs cap layer had to be optimized for V_{BD} and gm.

Device Fabrication

An epitaxial layer of the advanced pulse-doped structure as shown in Fig. 1-3-1 was successively grown by OMVPE. Thickness of the cap layer (xÅ) and the channel (yÅ) were designed to obtain Idss0 (Vg=0 V) of 250 - 350 mA/mm. After OMVPE growth, the active region was isolated by mesa etching. SiN film was deposited by p-CVD for passivation and

an annealing cap. To fabricate an LDD structure (Fig. 1-3-4), the n^+ ion-implanted (90 keV, 6E13 cm^{-2}) region was first defined by photoresist. Then, 0.7μm gates were fabricated by means of conventional photolithography based on dummy gate techniques. Self-aligned n' ion-implantation (120 keV, 4E12 cm^{-2}) was performed to reduce source resistance using an asymmetrical dummy gate with respect to the n+ region. After implantation, photoresist dummy gates were reduced by RIE and substituted with SiO_2 film. Rapid thermal annealing (840 °C, 2 seconds) was adopted for activation of the implanted Si. The AuGe/Ni ohmic metal was alloyed at 450 °C. The Ti/Pt/Au gate metal was overlapped on the SiO_2 film for the formation of a mushroom electrode. First and second metal interconnections consisting of Ti/Pt/Au were used to provide low resistance interconnects. The main process is similar to the technology described in the previous chapter.

• *NEW DEVICE STRUCTURE*

The key points to improve both the IM3 at the low and high back-off region simultaneously, are the adoption of the asymmetrical Lightly Doped Drain (LDD) structure shown in Fig. 1-3-5, the optimization of the distance and sheet resistance between the gate and drain electrode. Epitaxial layers of hetero GaAs MESFET with a pulse-doped channel were grown by OMVPE. The n' and n^+ implanted regions were formed by Si ion implantation and rapid thermal annealing.

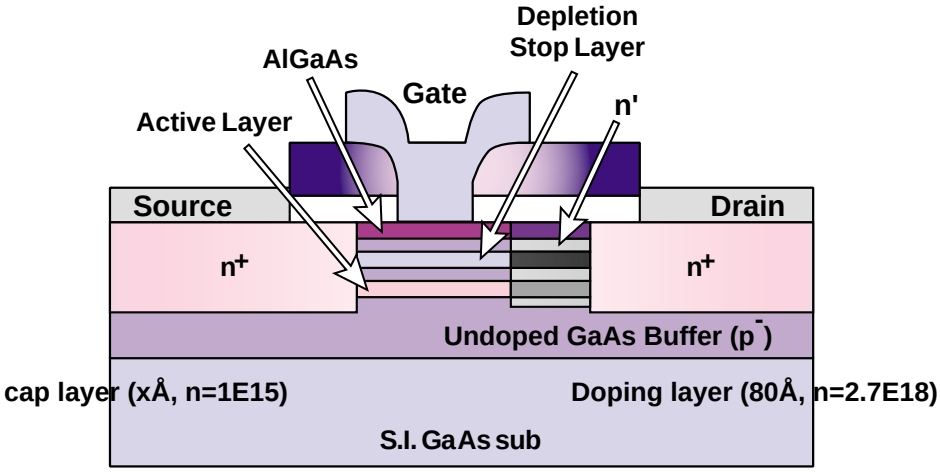

Fig. 1-3-5 : Structure of asymmetrical Lightly Poped Prain (LDD) FET

RF Power Performance of New LDD FET

Figure 1-3-6 shows the dependence of the saturated output power (Psat) and power added efficiency (PAE) on the drain voltage Vds for a conventional and an asymmetrical LDD structure. The Psat of an asymmetrical LDD FET is higher than that of a conventional FET, especially in the operating voltage of over 10V. This result shows that not only the on-resistance but also the gate-drain breakdown voltage are improved, because of extending the distance between the gate electrode and the edge of n^+ implanted region. The asymmetrical LDD FET delivered 905mW/mm at 15V operation by adopting an asymmetrical LDD structure. Fig. 1-3-7 shows the IM3 characteristics of a conventional and an asymmetrical LDD FET with a gate width of 20.8mm at high back-off. The IP3 of an asymmetrical LDD FET at the output power of 27dBm is 60.5dBm (P1dB+20dB) at class-A operation. The IM3 of the asymmetrical LDD FET is improved beyond 10dB for wide output power, due to suppressing the impact ionization phenomenon.

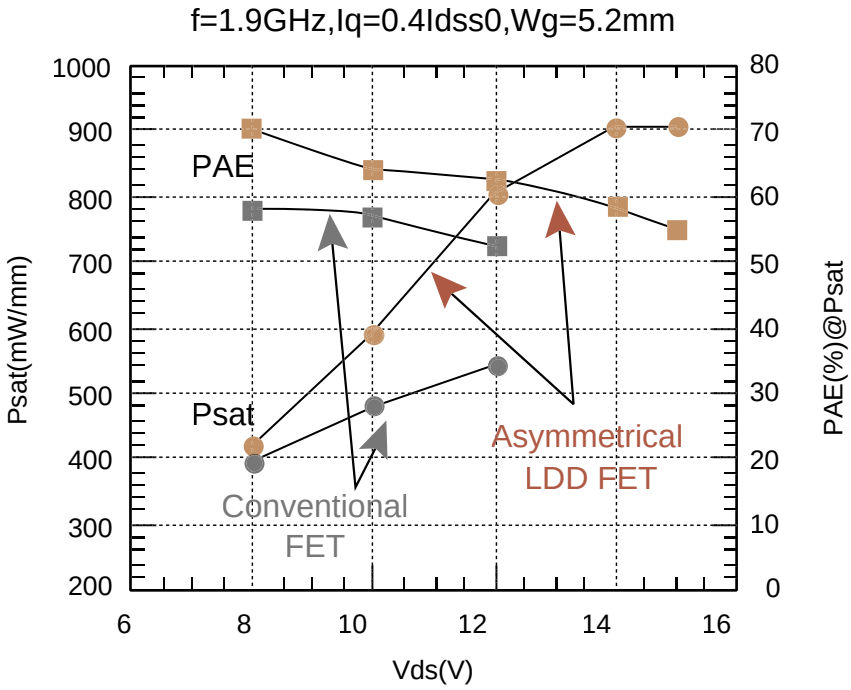

Fig. 1-3-6 : The dependence of the Psat and PAE on the drain voltage.

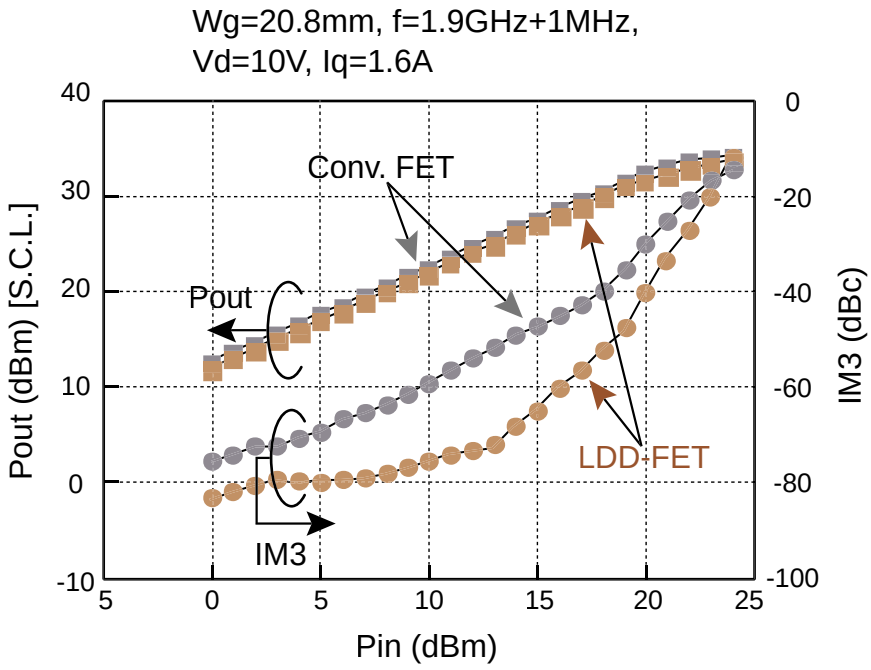

Fig. 1-3-7 : IM3 characteristics of conventional and asymmetrical LDD FET at high back-off. These data were tuned for IM3 at 10dB back-off from P1dB.